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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/006,406	11/30/2001	Bryan George Way	IDF 1239A (4000-04901)	4112
28003	7590	03/07/2006	EXAMINER	
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OVERLAND PARK, KS 66251-2100			2664	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/006,406	WAY ET AL.	
	Examiner	Art Unit	
	Chirag G. Shah	2664	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 24 February 2006.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-20 and 34 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-20 and 34 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 11/30/01 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Response to Arguments

1. Applicant's terminal disclaimer over U.S. Patent No. 6,343,079 has been fully considered. The nonstatutory double patenting rejection of claim 1 and 21-33 has been withdrawn.
2. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 1-9, 11-20 and 34 rejected under 35 U.S.C. 103(a) as being unpatentable over Pfeffer (U.S. Patent No. 6,128,293) in view of Riemann et al. (U.S. Patent No. 6,735,208), hereinafter referred as Riemann.

Regarding claim 1, Pfeffer discloses in fig. 1 of a PC (computer 26). It is inherent that a PC includes a central processor and a memory connected to the processor for operation. Pfeffer discloses in fig. 2 that a SAU 12 (multi-service card) attached to the PC 26, which clearly establishes that PC includes the bus interface, which connects to the CPU comprising a slot for attaching the multi-service card 12 to the PC 26.

Pfeffer discloses in fig. 2 of an autonomous multi-services card **[the multiservice access unit 12, see fig. 2]** is partially inserted into a slot means via path P4 to the PC clearly suggesting electronic communication with the bus interface of the PC, the that comprises:

a computer interface **[Ethernet interface 46, fig 2]** that is configured for coupling to a host computer connection (host computer includes a bus interface) and that is operational to exchange data with the host computer connection (bus interface in the host computer is inherent);

a telephone interface **[telephone interface 42, fig. 2]** that is configured for coupling to a telephone connection and that is operational to exchange voice signals with the telephone connection;

a network interface **[high speed modem 56, fig. 2]** that is configured for coupling to a network connection and that is operational to exchange the data and the voice signals with the network connection;

a communications processing system **[microprocessor 52, fig. 2]** that is operational to control the exchange of the voice signals with the telephone connection;

communication paths [**buses interconnecting the interfaces and the processor, see fig. 2]** that connect the communications processing system with the computer interface, the telephone interface, and the network interface; and

a substrate [**not shown but inherently disclosed**] that is configured for physical attachment to a computer 26 and that is connected to the computer interface, the telephone interface, the network interface, the communications processing system, and the communication paths. **Pfeffer further teaches that the network interface 56 is capable of accessing diverse communication networks, including, but not limited to, an ATM network, a PSTN (employing either ISDN, POTS, DSL etc.), Packet network (TCP/IP, X.25, Token ring etc.), and Frame Relay. The Pfeffer reference also describes the functions of all interfaces (42, 44, 46, and 48) and the processing system (52) as being claimed (see cols. 4 to 8).**

Pfeffer fails to disclose explicitly disclose a computer processing system operation without any control input from the central processor and to control the exchange of the data with the bus interface and with the network connection.

Riemann discloses in **fig. 3 and col. 7, lines 8-19** of client PC 18 equipped with a multi-port station module 30 having an ATM network interface 34, a conventional telephone station interface 32 and a DSP 33, control logic 36 and an (independent) control processor 38. Riemann clearly establishes based on col. 7, lines 40-65 that PC 18 includes the multi-port module 30 via PC bus 29, and the control processor 38 is capable of directing messages from network interface to another without the input control signal from the PC 18. Therefore, it would have been obvious to one of ordinary skills in the art at the time of the invention to modify the teachings of Pfeffer to include a multi-service card module that operates to process the network connection

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without any control input from the PC having the CPU. One is motivated as such in order to provide the predictable quality of service required for real-time bi-directional communication with reduced delay and increased performance.

Regarding claim 2, Pfeffer discloses wherein the computer 26 having the network interface [**high speed modem 56, fig. 2**] is further operational to exchange asynchronous transfer mode communications (see col. 5, lines 38-51 (**operational for ATM communication**) and col. 3, lines 45-67) with the network connection and wherein the communications processing system is further operational to control the exchange of the asynchronous transfer mode communications with the network connection [see col. 5, lines 15-50 and fig. 2, where **microprocessor controller 52 controls the exchange of ATM communication using high speed modem 56 of fig. 2**] as claim.

Regarding claim 3, Pfeffer discloses wherein the computer 26 having the network interface [**high speed modem 56, fig. 2**] is further operational to exchange Ethernet communications (**via Ethernet Interface 46, fig. 2**) with the network connection and wherein the communications processing system is further operational to control the exchange of the Ethernet communications with the network connection [see col. 5, lines 15-50 and fig. 2, where **microprocessor controller 52 controls the exchange of Ethernet communication using high speed modem 56 of fig. 2**] as claim.

Regarding claim 4, Pfeffer discloses wherein the computer 26 having the network interface [**high speed modem 56, fig. 2**] is further operational to exchange digital subscriber line communications (**PSTN of fig. 1 employing either ISDN, POTS, DSL etc., see col. 3, lines 45-58**), with the network connection and wherein the communications processing system is further operational to control the exchange of the digital subscriber line communications with the network connection [**see col. 5, lines 15-50 and fig. 2, where microprocessor controller 52 controls the exchange of DSL communication using high speed modem 56 of fig. 2**] as claim.

Regarding claim 5, Pfeffer discloses the computer 26 having wherein the network interface [**high speed modem 56, fig. 2**] is further operational to exchange Internet communications (**see col. 3, lines 14-30, full service provider server voice over data network**) with the network connection and wherein the communications processing system is further operational to control the exchange of the Internet communications with the network connection [**see col. 5, lines 15-50 and fig. 2, where microprocessor controller 52 controls the exchange of voice of data, Internet communication using high speed modem 56 of fig. 2**].

Regarding claim 6, Pfeffer discloses the computer 26 having wherein the computer interface [**Ethernet interface 46, fig 2**] is further operational to exchange Internet communications (**see col. 3, lines 14-30, full service provider server voice over data network**) with the host computer connection and wherein the communications processing system [**microprocessor 52, fig. 2**] is further operational to control the exchange Internet communications with the host computer connection [**see col. 5, lines 15-50 and fig. 2, where**

microprocessor controller 52 controls the exchange of voice of data, Internet communication using high speed modem 56 of fig. 2].

Regarding claim 7, Pfeffer discloses the computer 26 having wherein the telephone interface [**telephone interface 42, fig. 2]** is further operational to exchange analog telephone signals with the telephone connection and wherein the communications processing system [**microprocessor 52, fig. 2]** is further operational to control the exchange of the analog telephone signals with the telephone connection [see col. 3, lines 55-67, **fig. 2 and claim 2, where microprocessor controller 52 controls the exchange of analog telephone signals using high speed modem 56 of fig. 2].**

Regarding claim 8, Pfeffer discloses the computer 26 having wherein the network interface [**high speed modem 56, fig. 2]** is further operational to exchange modem communications with the network connection and wherein the communications processing system [**microprocessor 52, fig. 2]** is further operational to control the exchange of the modem communications with the network connection [see **fig. 2 and col. 5, lines 15-50, the microprocessor controls the exchange of modem 56 with ATM or PSTN network connection].**

Regarding claim 9, Pfeffer discloses the computer 26 having the network interface wherein the modem communications are cable modem communications [see **col. 4, lines 63 to col. 5, lines 5 and claim 3, digital modems equate to cable modems].**

Regarding claim 11, Pfeffer discloses the computer 26 having the network interface wherein the modem communications are telephone modem communications [see col. 4, lines 63 to col. 5, lines 5 and claims 3 and 4, the high speed modem may be analog or ISDN digital modem for voice call communication].

Regarding claim 12, the computer 26 having the network interface wherein the network interface is further operational to automatically sense the protocol used over the network connection [see, col. 6, lines 37-58 and col. 8, lines 25-35, the PRA interface 60, frame relay interface, packet interface and ATM interface provide protocol conversion functionality enabling dynamic rate and protocol adaptation].

Regarding claim 13, Pfeffer fails to disclose wherein the computer interface is further operational to receive power from the host computer connection. Riemann teaches of computer 18 having a client NIC 30 in fig. 3 including a switching power supply 35. The switching power supply is operational based on fig. 3 to receive power from the host computer pc 18. Therefore, it would have been obvious to one of ordinary skills in the art at the time of the invention to modify the teachings of Pfeffer to include the teachings of the NIC receiving power from host pc as taught by Riemann in order to facilitate communication transmission within the LAN.

Regarding claim 14, Pfeffer fails to disclose wherein the computer interface is further comprises a battery terminal. Riemann teaches of a computer 18 having a client network interface card (NIC) 30 in fig. 3 including a switching power/battery supply 35. The switching battery/power supply is operational based on fig. 3 to switching power. Therefore, it would have been obvious to one of ordinary skills in the art at the time of the invention to modify the teachings of Pfeffer to include the teachings of the NIC including a battery/power supply in order to facilitate communication transmission within the LAN.

Regarding claim 15, Pfeffer discloses further comprising a voice coder/decoder [see col. 4, lines 63-col. 5, lines 5, PCM voice encoding and decoding].

Regarding claim 16, Pfeffer discloses wherein the telephone interface [telephone interface 42, fig. 2] is operational to detect off-hook conditions, to detect on-hook connections, to detect tones, to provide dial tone, to provide ring current, to provide ringback tones, and to provide busy tones [see, col. 7, lines 24-37, telephone interface 42 detects off-hook conditions, DTMF detection and ringing signal generation among other controlling functionality].

Regarding claim 17, Pfeffer discloses wherein the communications processing system [microprocessor 52 of fig. 2] is operational to control the telephone interface to generate and receive telephone calls [see col. 7, lines 24-44, the microcontroller 52 operates to control the telephone interface 42 to originate and receive calls].

Regarding claim 18, Pfeffer fails to disclose the computer further comprising an enclosure wherein the central processor, the memory and the autonomous multi-service card are located within the enclosure. **Riemann discloses in fig. 3 of the PC 18 being equipped with the processor, multi-port module and control logic (memory).** Therefore, it would have been obvious to one of ordinary skills in the art at the time of the invention to modify the teachings of Pfeffer to include a multi-service card module inside of the PC as taught by Riemann. One is motivated as such in order to provide the predictable quality of service required for real-time bi-directional communication with reduced delay and increased performance.

Regarding claim 19, Pfeffer fails to disclose wherein the computer interface is wherein the enclosure includes a battery. Riemann teaches of computer having a computer 18 having a client NIC 30 in fig. 3 enclosure including a switching battery/power supply 35. The switching battery/power supply is operational based on fig. 3 to receive power. Therefore, it would have been obvious to one of ordinary skills in the art at the time of the invention to modify the teachings of Pfeffer to include the teachings of the NIC enclosure including a battery terminal as taught by Riemann in order to facilitate communication transmission within the LAN.

Regarding claim 20, Pfeffer discloses wherein: the network interface [**high speed modem 56, fig. 2**] is operational to exchange asynchronous transfer mode communications and internet communications with the network connection and wherein the communications processing system [**the microprocessor 52, see fig. 2**] is further operational to control the exchange of the asynchronous transfer mode communications and internet communications with

the network connection [see fig. 2 and col. 5, lines 15-50, the microprocessor 52 controls the exchange of modem 56 with ATM or Voice/Data Internet];

the telephone interface [telephone interface 42, fig. 2] is further operational to exchange analog telephone signals with the telephone connection and wherein the communications processing system [microprocessor 52, fig. 2] is further operational to control the exchange of the analog telephone signals with the telephone connection [see col. 3, lines 55-67, fig. 2 and claim 2, where microprocessor controller 52 controls the exchange of analog telephone signals using high speed modem 56 of fig. 2]; and

the computer interface [Ethernet interface 46, fig. 2] is further operational to exchange the Internet communications with the host computer connection and wherein the communications processing system [microprocessor 52, fig. 2] is further operational to control the exchange of the Internet communications with the host computer connection [see col. 5, lines 15-50 and fig. 2, where microprocessor controller 52 controls the exchange of voice of data, Internet communication using high speed modem 56 of fig. 2].

Regarding claim 34, Pfeffer disclose the computer 26 having an attached SAU 12 of fig. 2, wherein the bus interface 50 of fig. 2 is a peripheral component interconnect.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

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(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claim 10 rejected under 35 U.S.C. 103(a) as being unpatentable over Pfeffer in view of Riemann and further in view of Bender et al. (U.S. Pub No. 2003/0145119 A1), hereinafter Bender.

Regarding claim 10, Pfeffer in figure. 2 discloses of a high-speed modem 56 connected to terminal devices such as a Fax, PC, telephone etc. Pfeffer in-view of Riemann fails to explicitly disclose wherein the modem communications are wireless modem communications. Bender teaches of an interface between standard terminal equipment unit and high speed link. Bender discloses in fig. 3A of a wireless modem 42 connected to a terminal equipment unit for communication with other networks. Therefore, it would have been obvious to one of ordinary skills in the art to replace the high speed modem of Pfeffer in view of Riemann's system with a wireless modem as taught by Bender in order to ensure mobility for accessing the network from a remote location.

Conclusion

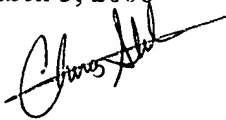
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chirag G. Shah whose telephone number is 571-272-3144. The examiner can normally be reached on M-F 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Huy Vu can be reached on 571-272-3155. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

cgs

March 3, 2006

A handwritten signature in black ink, appearing to read 'Chirag Shah', with a long horizontal stroke extending to the right.

Chirag Shah
Patent Examiner, AU 2616